Application Note

Preliminary data sheet TEA1085 listening-in circuit for line-powered telephone sets

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Summary:

The TEA1085 is a bipolar IC which has been designed for use in line powered telephone sets. It offers a listening-in facility for the received line signal via a loudspeaker.

Nearly all the line current can be used for powering the loudspeaker.

The circuit incorporates a supply circuit, a loudspeaker amplifier, a dynamic limiter, a MUTE circuit, a power down facility and logic inputs for gain setting.

Moreover a system called 'Larsen Level Limiter' is implemented that prevents annoying howling effects.

The IC is intended for use in conjunction with a transmission circuit of the TEA1060-family.

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- first version : ETT/AN8901, Febr. 1989
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GENERAL DESCRIPTION

The TEA1085 is a bipolar IC for use in line powered telephone sets. It offers a listening-in facility of the received line signal via a loudspeaker. The IC has to be applied in conjunction with a transmission circuit of the TEA1060-family.
It uses a part of the available line current via the internal supply circuit. The loudspeaker amplifier consists of a preamplifier, to amplify the earpiece signal from the transmission circuit and a double push-pull output stage to drive the loudspeaker in BTL (Bridge Tied Load) or SE (Single Ended) configuration.
To avoid high distortion of the loudspeaker signal, the gain of the preamplifier is controlled by a dynamic limiter. This is achieved by preventing signal clipping with respect to the available supply voltage and available supply current. Two logic inputs can be used to reduce the gain in 3 steps.
Due to acoustic feedback from the loudspeaker to the microphone annoying howling signals (Larsen effect) can occur on the telephone line and on the loudspeaker. As soon as the Larsen signal exceeds a voltage and time duration threshold, the Larsen Level Limiter (LLL) reduces the Larsen signal to a low level within a short time, by controlling the gain of the receiving preamplifier. The LLL uses the microphone signal as an input signal. Via a preamplifier and a 3-rd order filter the signal is processed in the LLL.
The MUTE input can be used to enable and disable the loudspeaker amplifier. It is provided with a toggle function to enable the use of a simple push-button switch.
By activating the power down (PD) input, the current consumption of the circuit will be reduced to enable pulse dialling or flash (register recall).
An internal start-circuit ensures normal start-up of the transmission-IC and start-up of the listening-in IC into standby condition.

FEATURES

* Internal supply
  - Optimum current split-up
    . Low constant current (adjustable) in transmission IC
    . Nearly all line current available for listening-in
  - Adjustable supply voltage
* Loudspeaker amplifier with:
  - Dynamic limiter providing low distortion and highest possible output power
  - SE or BTL drive of loudspeaker
  - Volume control by potentiometer and/or logic inputs (e.g. microcontroller drive)
  - Fixed gain (35dB)
* Larsen Level Limiter
  - Low sensitivity for own speech because of 3rd-order filter and attack delay
  - Adjustable voltage thresholds
* Power down input
* MUTE input with
  - Clickfree switching between listening-in mode and standby mode
  - Toggle function
  - Start-up in standby condition

PACKAGE OUTLINE:		
	TEA1085	24-lead dual in-line; plastic (SOT101B)
	TEA1085T	24-lead mini-pack; plastic (SO24, SOT137A)

REMARK: This preliminary data sheet contains advance information and is subject to change without notice.

QUICK REFERENCE DATA

parameter + conditions	symbol	min.	typ.	max.	unit
Input current range	I_{SUP}	4		120	mA
Stabilized supply voltage	V_{SUP}		3.60		V
Current consumption PD = HIGH	I_{SUP}		55		uA
Voltage gain loudspeaker amplifier SE	Gv		35		dB
BTL	Gv		41		dB
Max gain reduction with logic inputs (3 steps)	ΔGv		18		dB
Min. input current for an output power of					
Pout=20mW typ. into 50Ω SE	I_{SUP}		16		mA
Pout=40mW typ. into 50Ω BTL	I_{SUP}		32		mA
Larsen Limiter attack delay time v_{DTI} jumps from 0 to >=100mVrms	tad	100		200	msec
Larsen Limiter threshold level in Larsen mode	vDTI(rms)		7		mV
Larsen Limiter preamp gain setting range	Gv	30		52	dB
Operating ambient temperature range	Tamb	-25		+75	^{o}C

BLOCKDIAGRAM

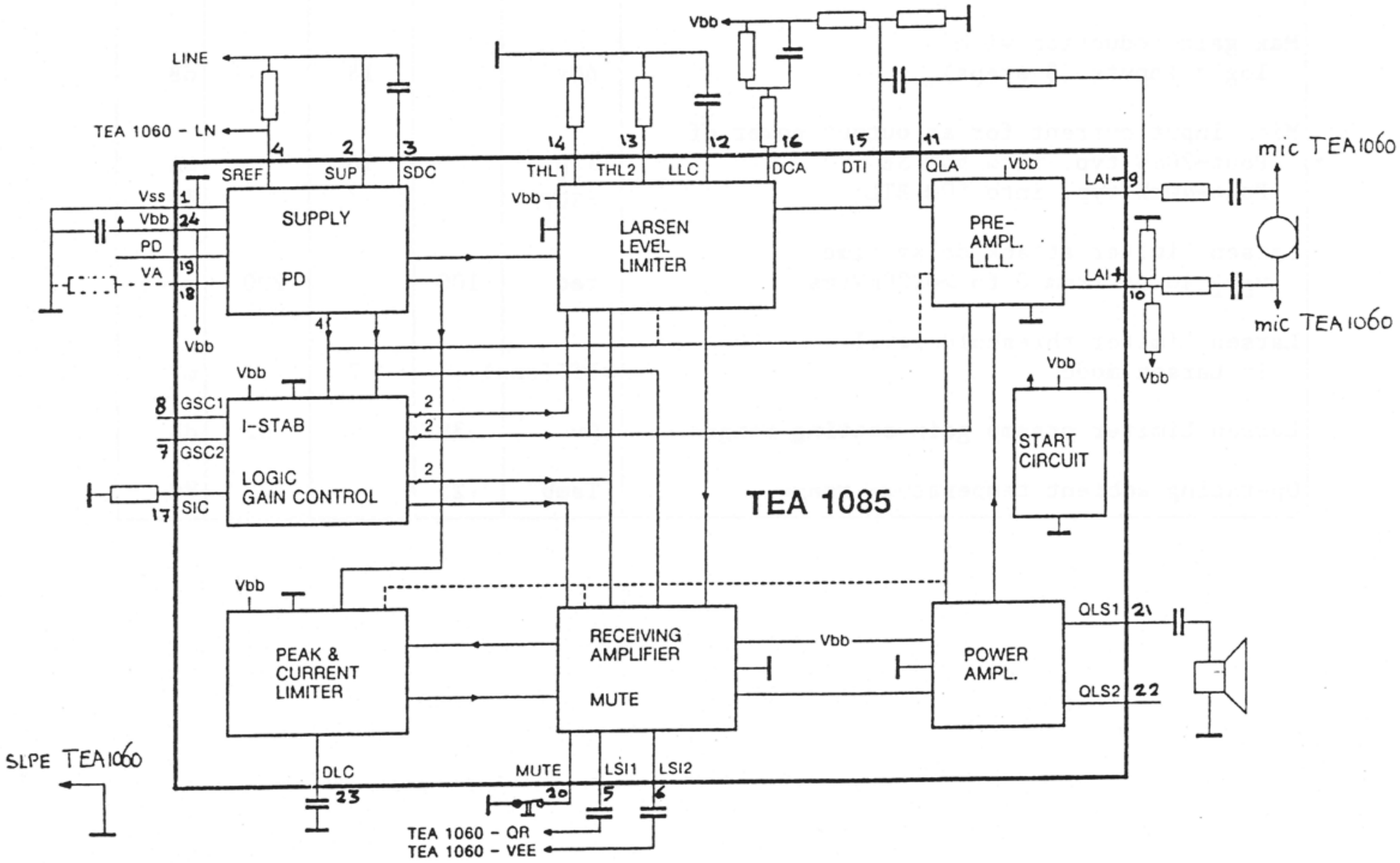


Fig.1. Blockdiagram of the TEA1085 with external components and connections to the transmission-IC.

PINNING

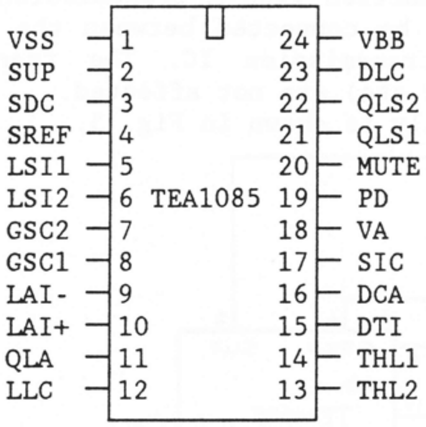


Fig.2. Pinning diagram.

1	VSS	Negative supply terminal
2	SUP	Positive supply terminal
3	SDC	Supply amplifier decoupling
4	SREF	Supply reference input
5	LSI1	Loudspeaker amplifier input 1
6	LSI2	Loudspeaker amplifier input 2
7	GSC2	Logic input 2 for gain select
8	GSC1	Logic input 1 for gain select
9	LAI-	Larsen limiter preamplifier inverting input
10	LAI+	Larsen limiter preamplifier non-inverting input
11	QLA	Larsen limiter preamplifier output
12	LLC	Larsen limiter capacitor
13	THL2	Larsen limiter residual threshold level
14	THL1	Larsen limiter attack delay threshold level
15	DTI	Larsen limiter detector input
16	DCA	Larsen limiter detector current adjustment
17	SIC	Larsen limiter current stabilizer
18	VA	VBB voltage adjustment
19	PD	Power down input
20	MUTE	Mute toggle input
21	QLS1	Loudspeaker amplifier output 1
22	QLS2	Loudspeaker amplifier output 2
23	DLC	Dynamic limiter capacitor
24	VBB	Decoupling of stabilized supply

FUNCTIONAL DESCRIPTION

GENERAL

The TEA1085 is normally applied in conjunction with a transmission circuit of the TEA1060-family. The circuit must be connected between the positive line terminal and pin SLPE of the transmission IC. The transmission characteristics (Impedance, gain settings etc) are not affected.
The interconnection with the TEA1060-family is shown in Fig. 3.

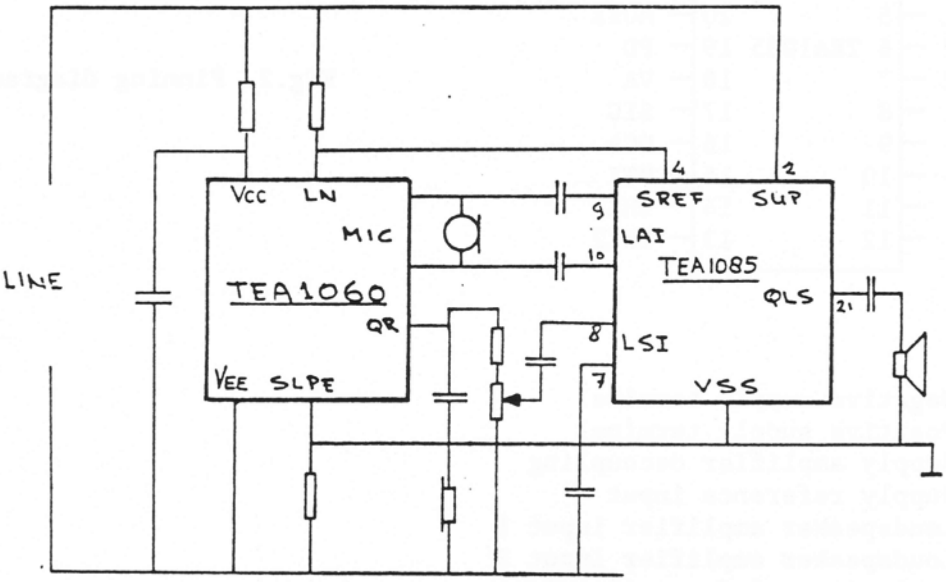


Fig. 3 Interconnection with TEA1060-family

SUPPLY (SUP, SREF, VBB, VSS, VA and SDC) pins 2, 4, 24, 1, 18 and 3.

The line current is split up into a current I_{TR} for the transmission IC and a current I_{SUP} for the listening-in circuit TEA1085. This is shown in Fig.4.

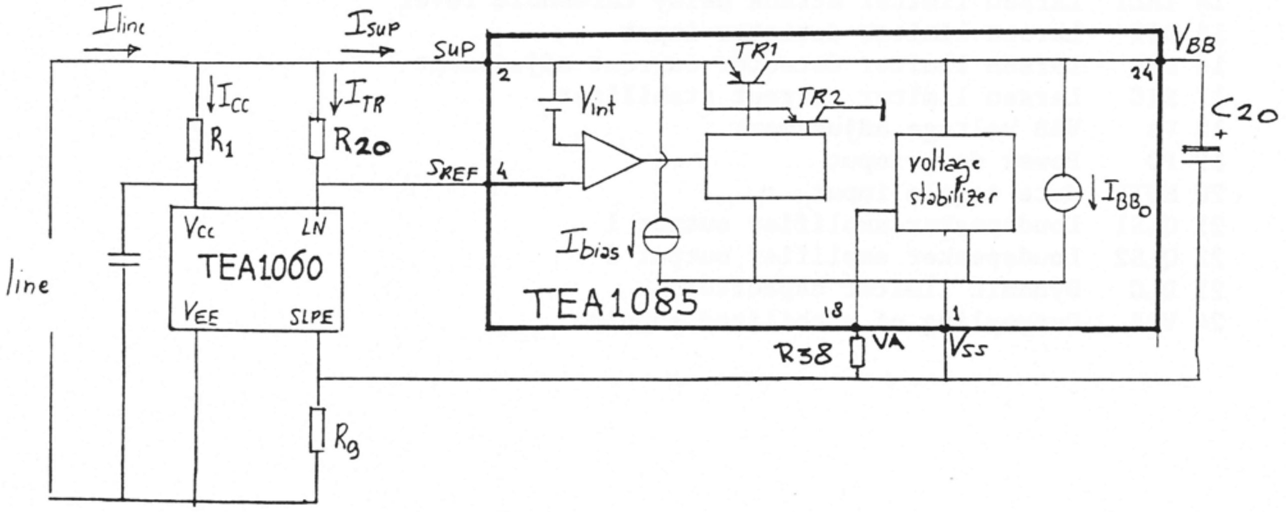


Fig. 4 Supply arrangement

I_{TR} is constant: I_{TR} = Vint/R20
I_{SUP} = Iline - Icc - I_{TR}.

in which
Vint is an internal temperature compensated reference voltage of typ. 300 mV between pins SUP and SREF.
R20 is a resistor between SUP and SREF
Icc is the internal current consumption of the TEA106X (≈ 1 mA)

A practical value for resistor R20 is 150 Ω. This yields I_{TR} = 2 mA and I_{SUP} = Iline - 3mA

The circuit stabilizes its own supply voltage at VBB. Transistor TR1 supplies the internal circuitry and TR2 minimizes line signal distortion by momentarily diverting input current to VSS whenever the instantaneous value of the voltage at SUP drops below the supply voltage VBB. VBB is fixed to typ. 3.6 V and can be increased by means of the external resistor R38 between VA and VSS.
The supply pin VBB is decoupled by means of C20 = 470 uF.

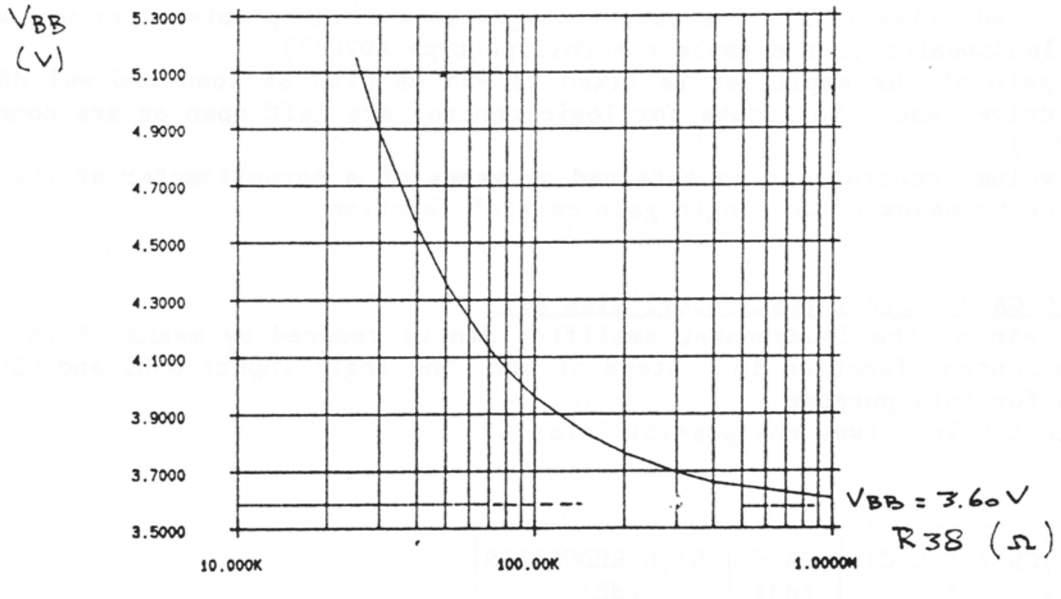


Fig.5 Stabilized supply voltage as a function of R38

The DC voltage V_{SUP} - VSS is determined by the transmission IC (hence $V_{LN-SLPE}$ of the TEA1060-family). So V_{SUP} - VSS = $V_{LN-SLPE}$ + Vint.
The minimum DC voltage that can be applied to the input is VBBmax + 0.4 V.

in which
VBBmax is the worst case max. supply voltage. This depends on the voltage setting by R38.

The internal current consumption of the TEA1085 (I_{SUPO}) is typically 4.2 mA at V_{SUP}-VSS = 4.5 V (mute=off). Hence the current available for powering the loudspeaker is $I_{SUP} - I_{SUPO}$. I_{SUPO} consists of a bias current of ≈0.4 mA for the circuitry connected to SUP and the current I_{BBO} (≈3.8 mA) used for the circuitry connected to VBB (see Fig. 4).

Stability:
Required are a 47pF capacitor between SDC and SUP, and a coil of 150μH between SUP and the positive line terminal (see fig. 16) to ensure stability of an application of the TEA1085 combined with a transmission IC of the TEA106X family.

LOUDSPEAKER AMPLIFIER (LSI1/LSI2 and QLS1/QLS2) pins 5/6 and 21/22.

The TEA1085 has symmetrical inputs LSI1, LSI2 for the receiving signal. The receiving signal is normally taken from the earpiece output of the transmission circuit via a resistive attenuator (See Fig. 3). The attenuation must be chosen according to the receive gain of the transmission IC (depends on the sensitivity of the earpiece transducer).
The maximum allowed input signal level is 450 mVrms at an ambient temperature of 25 °C.
The outputs QLS1 and QLS2 can be used for single ended drive (SE) or bridge tied load drive (BTL). The output stages have been optimised for use with a 50Ω loudspeaker (for example the Philips type AD2071).
The gain of the amplifier is fixed to ≈35 dB with SE load and ≈41 dB with BTL drive (when the inputs for logic control are left open or are connected to VSS).
The volume control can be obtained by means of a potentiometer at the input and/or by means of the logic gain control function.

LOGIC GAIN CONTROL (GSC1/GSC2) pins 8/7.

The gain of the loudspeaker amplifier can be reduced by means of the logic gain control function in 3 steps of 6dB. The logic inputs GSC1 and GSC2 are used for this purpose.
Table 1 below gives the possibilities.

GSC2	GSC1	GAIN (dB)	GAIN REDUCTION (dB)
0	0	35	0
0	1	29	6
1	0	23	12
1	1	17	18

Table 1. Data for microcontroller drive of GSC1/2 inputs.

"0" means connecting to VSS or leaving the pin open.
"1" means applying a voltage >= VSS + 1.5V.

DYNAMIC LIMITER PIN (DLC) pin 23.

To prevent distortion of the signal at the loudspeaker outputs QLS1 and QLS2, the gain of the amplifier is reduced rapidly when

a) the peaks of the signal at the loudspeaker outputs exceed an internally determined threshold (voltage limiter).
b) the DC current into SUP is insufficient (current limiter).
c) the voltage at VBB decreases below an internally determined threshold (typ 2.9V) (VBB limiter).

The time in which gain reduction is effected is called the attack time. This is very short in cases a) and c) and relatively long in case b). The circuit stays in the gain-reduced condition until the peaks of the output signal remain below the threshold level. The gain then returns to nominal level after a time (release time) determined by capacitor C28 connected to DLC.

MUTE input (MUTE) pin 20.

The mute function is intended to switch over between stand-by condition and listening-in condition. The mute circuit is provided with a toggle function. Switching occurs by means of the positive edges of the signal at the MUTE pin (see Fig. 6).

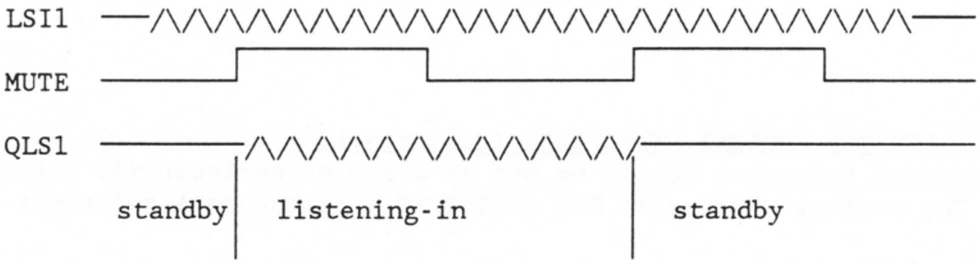
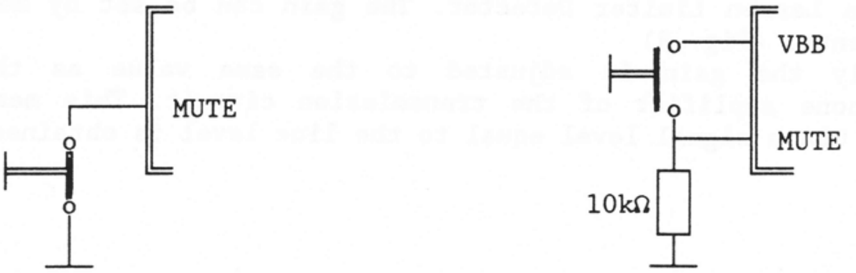


Fig. 6 Behaviour of MUTE 'toggle'-function.

Normally the MUTE pin must be LOW (connected to VSS).
A simple push-button switch can be used to operate the MUTE toggle (See Fig. 7). Debouncing can be realized by means of a small capacitor between MUTE and VSS.
An internal start-circuit ensures that the circuit always starts up in standby condition.



a) 'break' contact b) 'make' contact

Fig. 7 Alternative possibilities to connect a switch to the MUTE

POWER DOWN input (PD) pin 19.

During pulse dialling or register recall (timed loop break) the telephone line is interrupted; as a consequence it provides no supply for both the transmission circuit and the listening-in circuit. The supply gap for the listening-in circuit has to be bridged by the charge of capacitor C20 connected at VBB.
By applying a HIGH level to the PD input during the time of the loop break the requirement on this capacitor is eased. This reduces the internal (standby) current consumption (I_{BBO} in Fig. 4) at VBB from (typ.) 3.8mA to (typ.) 400μA. In order not to affect the behaviour of the transmission circuit the transistors TR1 and TR2 are blocked and also the bias current flowing into SUP is reduced from ≈0.4mA to ≈55μA with VSUP=4.5V according the following equation.

$$I_{SUP(PD)} = I_{BIAS(PD)} = (V_{SUP} - 2Vd)/Ra \quad (\text{when } 4.2 < V_{SUP} < VBB + 3\ V)$$

in which:
2Vd is the voltage drop across 2 internal diodes (about 1.3V)
Ra is an internal resistor of typ. 60 kΩ.

LARSEN LIMITER CURRENT STABILIZER (SIC) pin 17.

The current reference has to be set by means of resistor R36 between SIC and VSS. The preferred value of R36 is 120 kΩ. The internal reference current:

$$I_{SIC} = \frac{1.25}{R36} \quad \text{with R36 = 120 k}\Omega \text{ this yields } I_{SIC} = 10.4\mu A.$$

Changing R36 will affect the timing of the Larsen Level Limiter system.

LARSEN LIMITER PREAMPLIFIER (LAI-/LAI+ and QLA) pins 9/10 and 11.

This circuit amplifies the microphone signal to a sufficiently high level for the Larsen Limiter Detector. The gain can be set by means of external components. (Fig. 8)
Normally the gain is adjusted to the same value as the gain of the microphone amplifier of the transmission circuit. This means that at the output QLA a signal level equal to the line level is obtained.

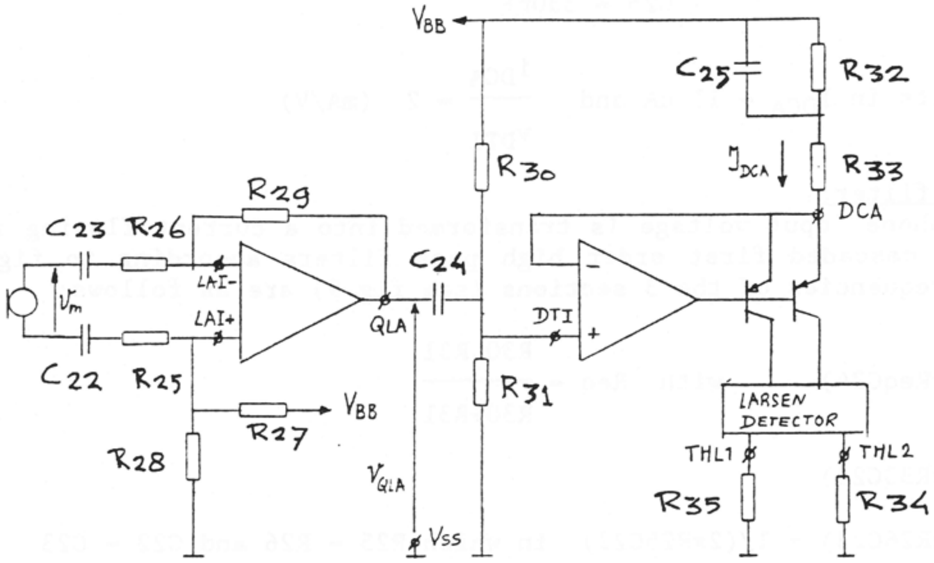


Fig. 8 Larsen limiter preamp and V/I converter

The gain between QLA and micr. input is given by: (the high pass filter is not taken into account)

$$\text{Apre} = \frac{v_{QLA}}{v_m} = R29/R26$$; in the basic application R25 = R26 = 10kΩ

The gain can be adjusted between 30 dB (R29 = 316kΩ) and 52 dB (R29 = 4MΩ). For the bias resistors R27 and R28 is required: R27 = R28 = 2 * R29.

LARSEN LIMITER DETECTOR (DTI and DCA) pins 15 and 16.

The QLA output signal is AC coupled to the detector input DTI. The input DTI is biased by means of the two external resistors R30 and R31.
The voltage applied to pin DTI of the Larsen Limiter Detector is converted into a current for further processing in the Larsen Level Limiter. The adjustment of current is done by means of the network between DCA and VBB. (See Fig. 8).
This current is:
For DC:

$$I_{DCA} = \frac{R30}{R30+R31} * V_{BB} * \frac{1}{R32+R33}$$

For AC:

$$i_{DCA} = \frac{v_{DTI}}{R33} \qquad \text{for } f \gg 1/(2\pi R33C25)$$

In the basic application: R30 = 100kΩ, R31 = 220kΩ, R33 = 500 Ω, R32 = 100kΩ
C25 = 330nF

This results in I_{DCA} = 11 uA and $\frac{i_{DCA}}{v_{DTI}} = 2$ (mA/V)

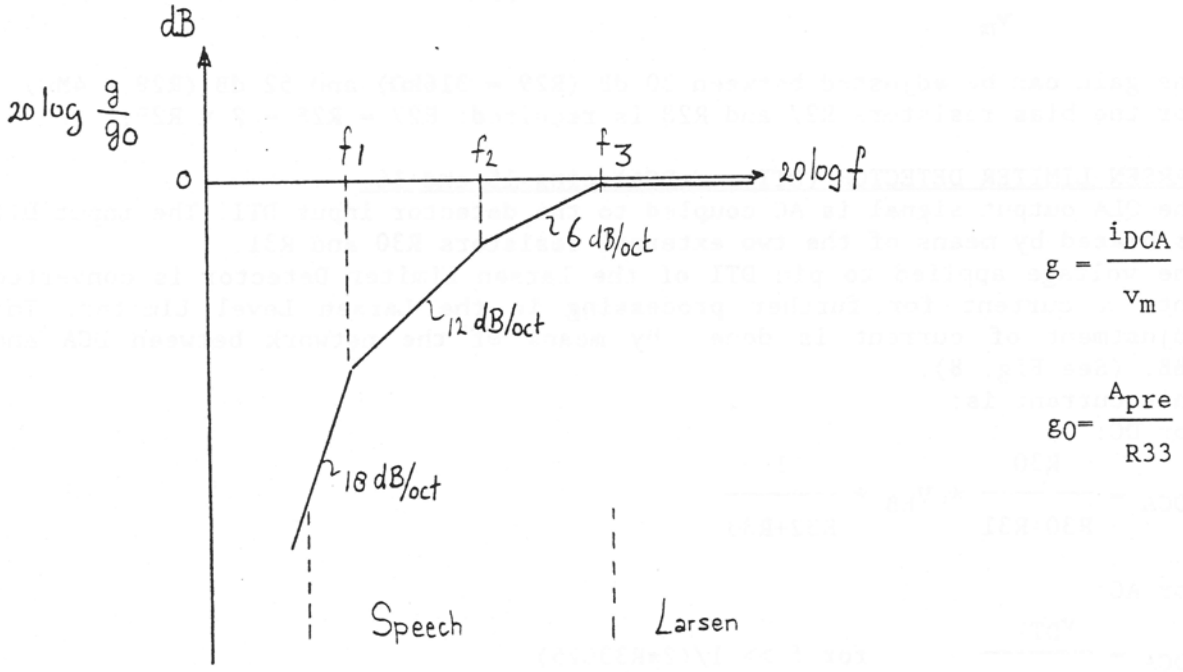
High pass filter:
The microphone input voltage is transformed into a current flowing into DCA via three cascaded first order high pass filters according to fig.8. The cut-off frequencies of the 3 sections (see fig.9) are as follows:

$$f1 = 1/(2\pi ReqC24) \qquad \text{with} \quad Req = \frac{R30\ R31}{R30+R31}$$

$$f2 = 1/(2\pi R33C25)$$

$f3 = 1/(2\pi R26C23) = 1/(2\pi R25C22)$ in which R25 = R26 and C22 = C23.

This filter reduces the sensitivity of the system to own speech. Normal speech is in the frequency range 300Hz - 3400Hz; Larsen signal normally occurs at a frequency > 3kHz.
With the component values used in the basic application (see Fig. 16):
f1= 500Hz, f2 = 1kHz, f3 = 3kHz.



$$g = \frac{i_{DCA}}{v_m}$$

$$g_0 = \frac{A_{pre}}{R33}$$

Fig. 9 Third order high pass filter (cascaded).

LARSEN LIMITER CAPACITOR (LLC) pin 12.

An external capacitor must be connected between LLC and VSS (C26 = 1 uF in the basic application). This capacitor determines timing (attack and release times) of the Larsen Level Limiter in both the listen-in mode and Larsen mode (see chapters: Listen-in and Larsen mode). The timing is also dependent on the value of R36 which is connected between SIC and VSS.

LARSEN LEVEL LIMITER THRESHOLD (THL1/THL2) pins 14/13.

As soon as the signal at DTI exceeds a first threshold , the Larsen Level Limiter starts discharging the larsen limiter capacitor C26. This first threshold is determined by resistor R35 between THL1 and VSS. The discharge of C26 depends on how much the signal at DTI exceeds the first threshold. For normal speech the discharge will be small.
Larsen effect generally is defined as a signal level on the line of 100mVrms or more that lasts for more than 100msec. The Larsen signal must be reduced to a low level within 200msec (CNET requirement). For Larsen signal levels (f>f3 in Fig. 9) of 100mVrms or more at the input DTI, and with the component values used in the basic application, the system will switch from listen-in mode to Larsen mode in a time between 100msec and 200msec. In this way the initial Larsen effect that will occur will last for only a short time. This reaction time is called: the 'attack delay time' (tad). The attack delay time ensures little sensitivity of the system for own speech.

The first threshold at DTI is determined by:

$$V_{DTI1} = \left(\frac{1.25}{R35} - \frac{I_{DCA}}{2}\right) * 2 * R33 \qquad \text{(if f > f3 in Fig. 9)}$$

in which I_{DCA} = the DC current into pin DCA

With the component values of the basic application (see Fig. 16), I_{DCA} = 11 uA. This yields V_{DTI1} = 18.8 mV

Listen-in mode

In case of normal speech the discharge of the capacitor connected to LLC will not be sufficient to reach the threshold level where the system switches to Larsen mode. This because normal speech is not continuous, the discharge of C26 is rather slow (attack delay) and the charge time is relatively fast.

The slope of V_{LLC} during charge in listen-in mode:

$$Sli = \frac{\partial V_{LLC}}{\partial t} = \frac{1.25}{C26*R36} \qquad \text{(V/sec)}$$

With C26 = 1uF and R36 = 120kΩ this results in Sli = 10 V/sec.

Discharge of the capacitor at LLC takes place during the times where the signal at DTI exceeds V_{DTI1}. Hence for a continuous signal at DTI; the attack delay time tad (see Fig. 10) is determined by:

$$tad = \frac{C26 * R36}{2 * (3 * k - 1)}$$

in which k = tl/T (duty cycle) is determined by the time in which the first threshold (V_{DTI1}) is exceeded by the signal at pin DTI. (See Fig. 11). Hence k <= 0.5 (large signals)

and with the component values of the basic application:
k >= 0.457 for signals >= 100mVrms

This yields tad <= 160 msec \ for v_{DTI} >= 100 mVrms
tad >= 120 msec /

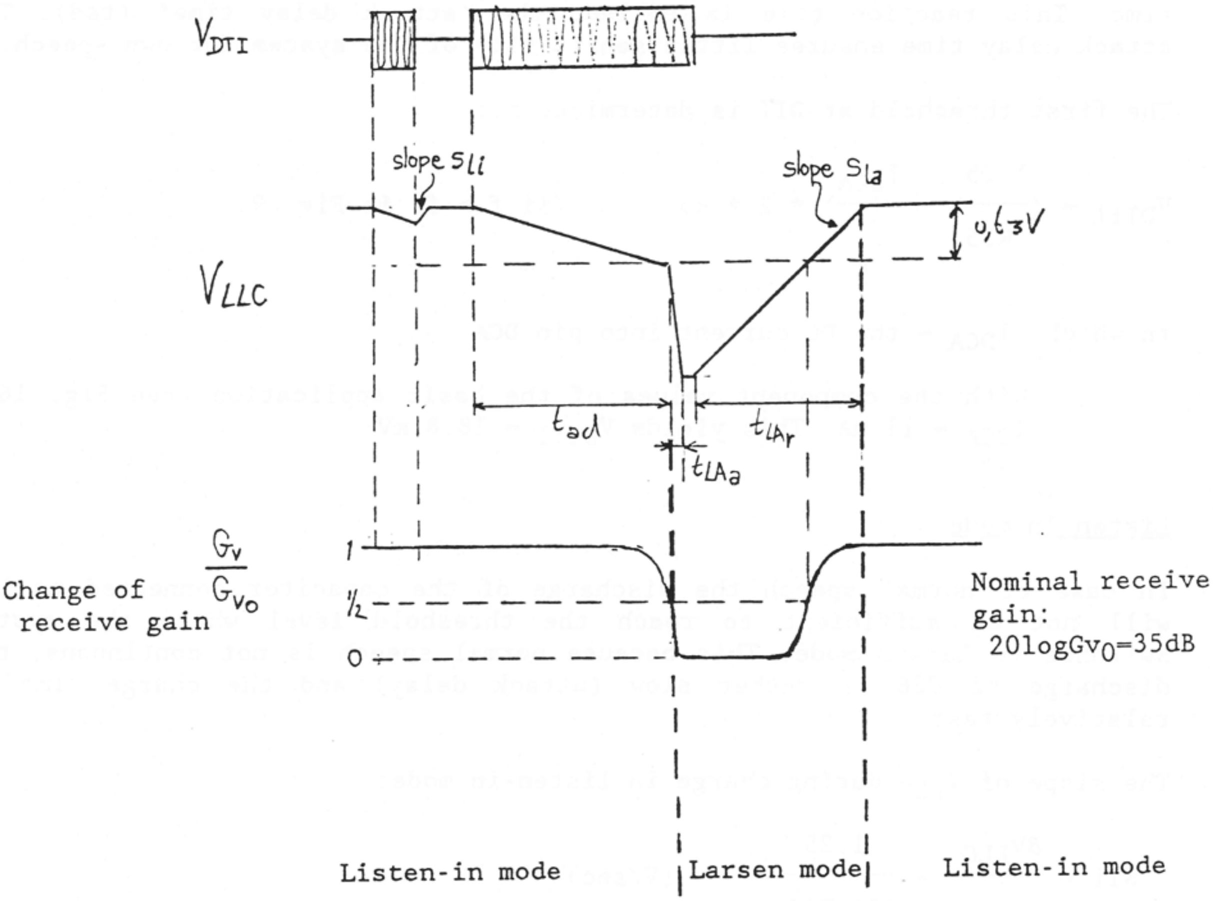
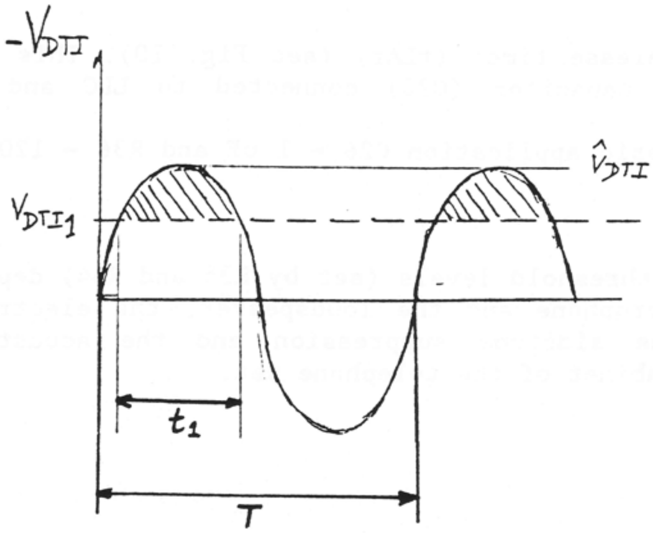


Fig. 10 Dynamic behaviour of Larsen limiter (in open loop condition).



$$k = \frac{t_1}{T}$$

$$k = 0.5 - \frac{\arcsin\left(\frac{V_{DTI1}}{\hat{v}_{DTI}}\right)}{\pi}$$

Fig. 11 Definition of duty cycle k.

Larsen mode

After the 'attack delay time', the circuit switches from listen-in mode to the 'Larsen mode'. The gain of the loudspeaker amplifier is then reduced quickly (tLAa = Larsen attack time in Fig. 10) to such a value that the residual Larsen signal will be determined by a second threshold. This second threshold can be set by means of R34 between pin THL2 and VSS. The second threshold must be selected always at a lower level than the first threshold; therefore R34 > R35.
The time in which the gain reduction is effected (tLAa) is very short.
In the 'Larsen mode' the circuit acts as a dynamic limiter with peak detector and regulates the gain in such a way that the signal level at DTI is determined by the second threshold VDTI2.

The second threshold at DTI is determined by:

$$V_{DTI2} = \left(\frac{1.25}{R34} - \frac{I_{DCA}}{2}\right) * 2 * R33 \qquad \text{(if f > f3 in Fig. 9)}$$

with the component values of the basic application (see Fig. 16) this yields $V_{DTI2} = 6.9$ mV.

The charge current in larsen mode is reduced to half of the charge current in listen-in mode.
The slope of the voltage at LLC during charge in Larsen mode (see Fig. 10):

$$Sla = \frac{\partial V_{LLC}}{\partial t} = \frac{1.25}{2*C26*R34} \qquad \text{(V/sec)}$$

With the component values used in the basic application: Sla = 5 V/sec.

When the Larsen effect stops (when the total open loop gain < 1), the gain of the loudspeaker amplifier will return to its normal value in a time

period know as the 'Larsen release time' (tLAr) (see Fig. 10). This time period is determined by the capacitor (C26) connected to LLC and the resistor (R36) at SIC.
With the values used in the basic application C26 = 1 uF and R36 = 120 kΩ: tLAr = 250msec.

In practice the choice of the threshold levels (set by R35 and R34) depends on the sensitivity of the microphone and the loudspeaker, the electrical gains (sending, receive), the sidetone suppression and the acoustical properties determined by the cabinet of the telephone set.

RATINGS Limiting values in accordance with the Absolute Maximum System(IEC134)

parameter	symbol	min.	max.	unit
Positive voltage on SUP				
continuous	VSUP		12	V
during switch-on or line interruption	VSUP		13.2	V
Repetitive voltage on SUP during 1msec/5sec with current limiting resistor of 12 Ω in series with SUP	VSUP		28	V
Voltage on SREF	VSREF	VSS-0.5	VSUP+0.5	V
Voltage on all other pins	V	VSS-0.5	VBB+0.5	V
Current into SUP TEA1085	ISUP		120	mA (Fig.12)
TEA1085T	ISUP		120	mA (Fig.13)
Power dissipation (Tamb=75°C; Tj=125°C)				
TEA1085	Ptot		1	W
TEA1085T	Ptot		666	mW
Storage temperature	Tstg	-40	+125	°C
Operating ambient temperature range	Tamb	-25	+75	°C
Junction temperature	Tj	-	+125	°C

THERMAL RESISTANCE

From junction to ambient in free air

TEA1085	Rthj-a	typ.	50	K/W
TEA1085T mounted on a glass-epoxy board of 40.1 x 19.1 x 1.5 mm	Rthj-a	typ.	75	K/W

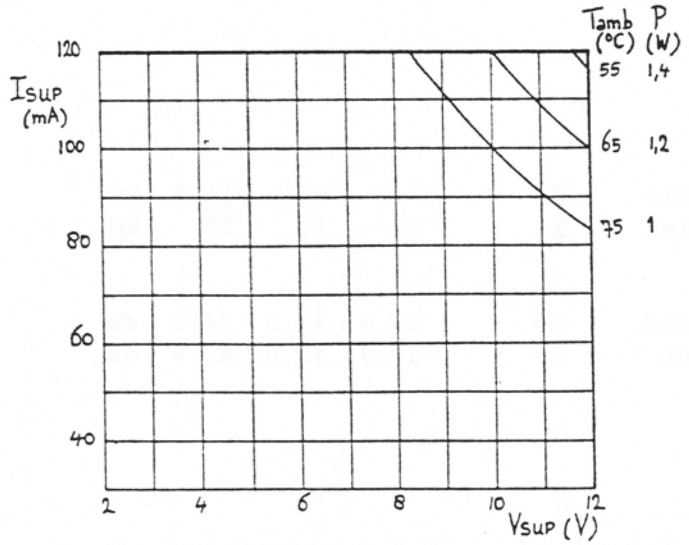


Fig. 12 TEA1085 Safe operating area.

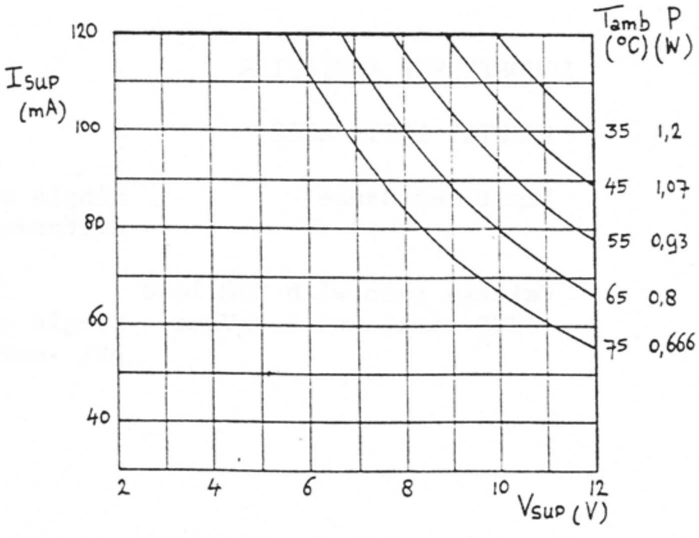


Fig. 13 TEA1085T Safe operating area.

CHARACTERISTICS

V_{SREF} = 4.2V, VSS = 0 V, I_{SUP} = 15mA, v_{SUP}= 0, f=800 Hz, Tamb = 25 °C; PD = LOW; MUTE = off (listen-in condition); GSC1=GSC2=LOW; 50Ω loudspeaker; no R38; testcircuit in Fig. 14; unless otherwise specified

parameter + conditions		symbol	min.	typ.	max.	unit
SUPPLY						
Minimum DC input voltage		VSUP	-	VBB_{typ}+0.7	-	V
Internal reference voltage		VSUP-SREF	275	315	355	mV
Stabilized supply voltage						
No R38	ISUP=15mA	VBB	3.40	3.60	3.80	V
variation at ISUP= 15 to 120mA		ΔVBB	-	10	-	mV
With R38=39 kΩ connected between VA and VSS, V_{SREF}=5.2V	ISUP=15mA	VBB	4.20	4.45	4.70	V
Variation with temperature No R38, Tamb=-25 to 75°C, ISUP=15mA		ΔVBB/ΔT	tbf	-0.2	tbf	mV/K
Minimum operating current		ISUP	-	4.2	tbf	mA
Distortion of AC signal on SUP	$V_{SUP(rms)}$=1V	THD	-	0.3	2	%
Noise between SUP-VEE		vno(rms)	-	-72	-	dBmp
Current consumption in power down condition PD = HIGH, VSUP = 4.5 V		ISUP	-	55	75	µA
	VBB = 3.60V	IBB	-	400	tbf	uA
LOUDSPEAKER AMPLIFIER						
INPUTS: LSI1, LSI2						
Input impedance	Single ended	Zi	7.5	9.5	11.5	kΩ
	differential	Zi	15	19	23	kΩ
Voltage gain with 50Ω load ISUP=15mA, vi=1.8mVrms	Single ended	Gv	34.0	35.0	36.0	dB
	BTL -output	Gv	39.9	40.9	41.9	dB

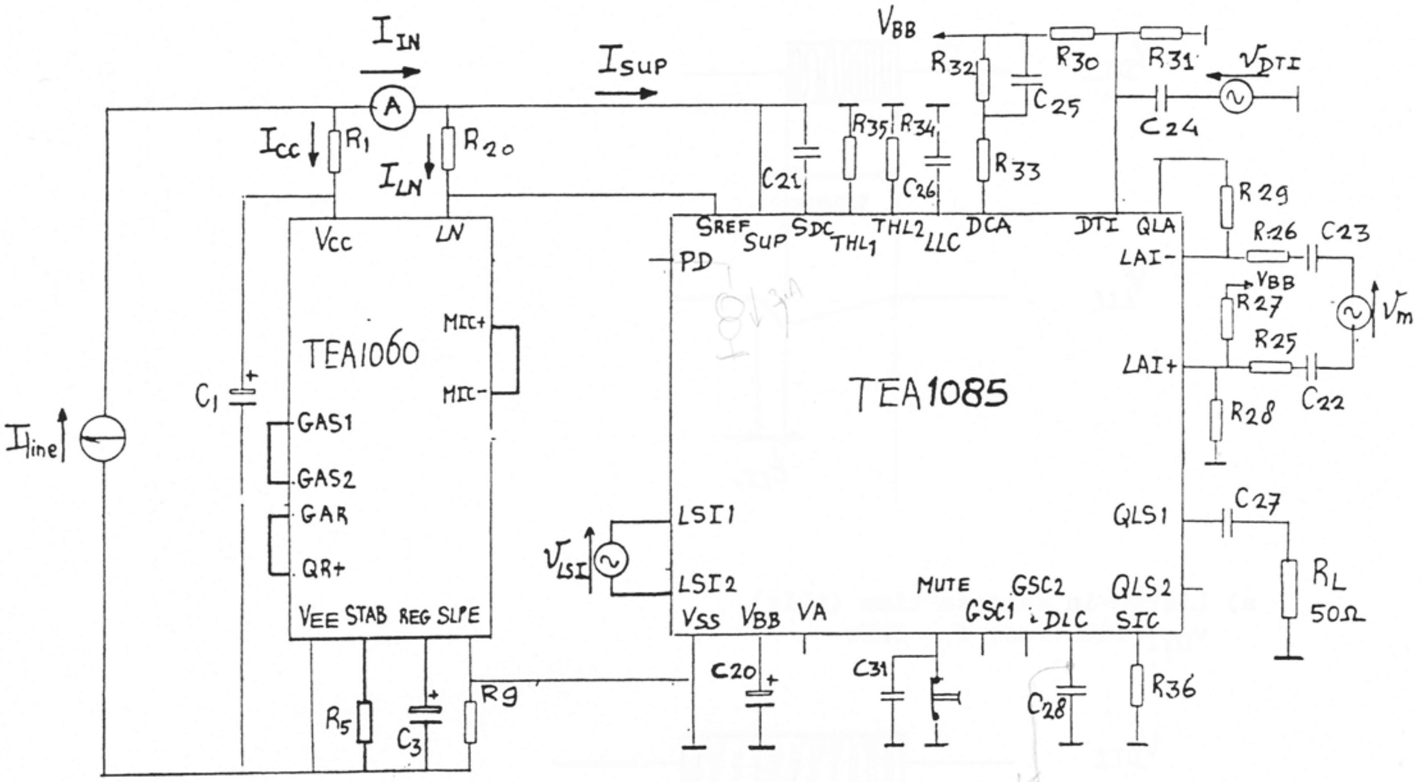
parameter + conditions		symbol	min.	typ.	max.	unit
Variation with signal level						
vi= 1.8mVrms and 14mVrms	Single ended	ΔGv	-	0.1	0.4	dB
ISUP = 50 mA	BTL -output	ΔGv	-	0.2	0.4	dB
Variation with frequency referred to 1kHz						
f = 300 and 3400 Hz	Single ended	ΔGv	-	±0.1	-	dB
vi= 1.8mVrms	BTL -output	ΔGv	-	±0.1	-	dB
Variation with temperature referred to 25 °C						
Tamb = -25 to + 75 °C	Single ended	ΔGv	-	±0.4	-	dB
	BTL -output	ΔGv	-	±0.5	-	dB
LOUDSPEAKER OUTPUTS: QLS1 QLS2						
Output capabilities						
Output voltage with vi=22mVrms						
ISUP = 9 mA	SE	Vo(p-p)	1.2	1.45	-	V 1)
ISUP = 16 mA	SE	Vo(p-p)	2.5	2.9	-	V 2)
ISUP = 23.5mA	BTL	Vo(p-p)	2.5	2.9	-	V 2)
ISUP = 32 mA	BTL	Vo(p-p)	3.5	4.0	-	V 3)
Total harmonic distortion with vi=22mVrms						
ISUP = 9 mA	SE	THD	-	0.4	2	%
ISUP = 16 mA	SE	THD	-	0.7	2	%
ISUP = 23.5 mA	BTL	THD	-	0.4	2	%
Output voltage with vi=22mVrms, ISUP=16mA; $V_{SUP-VEE}$=1Vrms	SE	Vo(p-p)	2.2	2.55	-	V

1) typ. 5 mW output power
2) typ. 20mW output power > into 50 Ω
3) typ. 40mW output power

parameter + conditions		symbol	min.	typ.	max.	unit
Dynamic limiter						
Total harmonic distortion with vi=22mVrms + 10dB						
ISUP = 9 mA	SE	THD	-	0.5	10	%
ISUP = 16 mA	SE	THD	-	1.2	10	%
ISUP = 23.5 mA	BTL	THD	-	0.6	10	%
Dynamic behaviour of limiter SE-load						
Attack time, vi jumps from 10mVrms to 65mVrms						
Voltage limiter	ISUP = 17 mA	tatt	-	2	5	msec
Current limiter	ISUP = 12 mA	tatt	-	500	tbf	msec
VBB limiter	ISUP = 9 mA	tatt	-	tbf	tbf	msec
Release time, vi jumps from 65mVrms to 10mVrms	ISUP = 17 mA	trel	tbf	75	tbf	msec
Threshold VBB-limiter VBB level below which gain reduction starts	ISUP = 9 mA	VBBo	tbf	2.9	tbf	V
Noise output voltage with 1kΩ between inputs LSI1, LSI2; psophometrically weighted (P53 curve)	SE	Vno(rms)	-	170	-	μV
	BTL	Vno(rms)	-	350	-	μV
LOGIC GAIN CONTROL						
	GSC2 GSC1					
Reduction of voltage gain	0 1	ΔGv	5.5	6	6.5	dB
	1 0	ΔGv	11.5	12	12.5	dB
	1 1	ΔGv	17	18	19	dB
LARSEN LIMITER PREAMPLIFIER						
Opamp characteristics						
Open loop gain		Gv0	-	92	-	dB
1st pole		fp1	-	120	-	Hz
2nd pole		fp2	-	3.3	-	MHz
Unity gain bandwidth		GB	-	4	-	MHz

parameter + conditions	symbol	min.	typ.	max.	unit
Voltage gain at f = 3 kHz R26= 10kΩ R29=4MΩ	Gv	51.5	52.0	52.5	dB
Gain adjustment range	Gv	30	-	52	dB
LARSEN LIMITER DETECTOR					
V to I converter:					
DC offset voltage at VBB-VDTI = 1V	VDCA-VDTI	-25	1.0	25	mV
Voltage gain from DTI to DCA with v_{DTI}=100mV(rms); f=3kHz	Gv	tbf	-0.8	tbf	dB
DC voltage at THL1 R35=51kΩ	VTHL1	1.18	1.25	1.33	V
DC voltage at THL2 R34=100kΩ	VTHL2	1.18	1.25	1.33	V
Dynamic behaviour with a burst at input DTI; f=3kHz; test signals in Fig.15					
Listen-in release time (fig.15a)	tLIr	tbf	40	tbf	msec
Attack delay time (fig.15b)					
vDTI jumps from 0 to 100mVrms	tad	-	160	200	msec
vDTI jumps from 0 to 1Vrms	tad	100	120	-	msec
Larsen attack time (fig.15b) vDTI = 100mVrms	tLAa	-	20	tbf	msec
Larsen release time (fig.15b) vDTI jumps from 100mVrms to 0mV	tLAr	tbf	250	tbf	msec
DC-voltage at LLC; vDTI = 0	$VLLC_0$	1.8	1.9	2.0	V
VLLC reduction to attack Larsen Mode	-ΔVLLC	0.59	0.63	0.68	V
Gain reduction with VLLC=0.7V	ΔGv	60	tbf	tbf	dB

parameter + conditions	symbol	min.	typ.	max.	unit
MUTE INPUT (toggle function, positive edge triggered set-reset flipflop)					
Input voltage LOW	VIL	0	-	0.3	V
Input voltage HIGH	VIH	1.5	-	VBB+0.4	V
Input current at MUTE=0	Imute	-	-22	-28	μA
Min. input pulse width	t_M	-	50	-	μsec
Min. pulse repetition time	T_R	-	2	-	msec
Supply voltage below which MUTE-toggle is reset	VBBm	-	2	-	V
Reduction of gain from LSI1, LSI2 to QLS1 or QLS2 with MUTE = on	ΔGv	60	100	-	dB
POWER DOWN INPUT PD					
Input voltage LOW	VIL	0	-	0.3	V
Input voltage HIGH	VIH	1.5	-	VBB+0.4	V
Input current at MUTE=HIGH	IPD	-	2.3	2.8	μA
LOGIC INPUTS GSC1, GSC2					
Input voltage LOW	VIL	0	-	0.3	V
Input voltage HIGH	VIH	1.5	-	VBB+0.4	V
Input current at GSC1/2 = HIGH	IGSC	-	6	8	μA



The DC current split up:

$$I_{SUP} = I_{IN} - \frac{V_{SUP-SREF}}{R20} \qquad I_{LN} = \frac{V_{SUP-SREF}}{R20}$$

Component values:

R1 = 620Ω
R5 =3.6kΩ
R9 = 20Ω

R20 = 150Ω
R25 = 10kΩ
R26 = 10kΩ
R27 = 8MΩ

R28 = 8MΩ
R29 = 4MΩ
R30 = 100kΩ
R31 = 220kΩ
R32 = 100kΩ
R33 = 500Ω
R34 = 100kΩ
R35 = 51kΩ

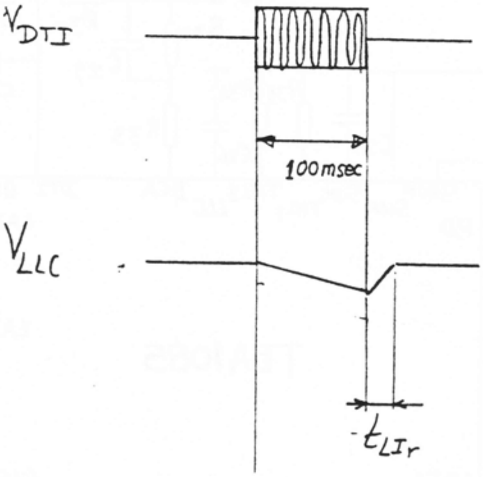
R36 = 120kΩ

C1 = 100μF
C3 = 4.7μF

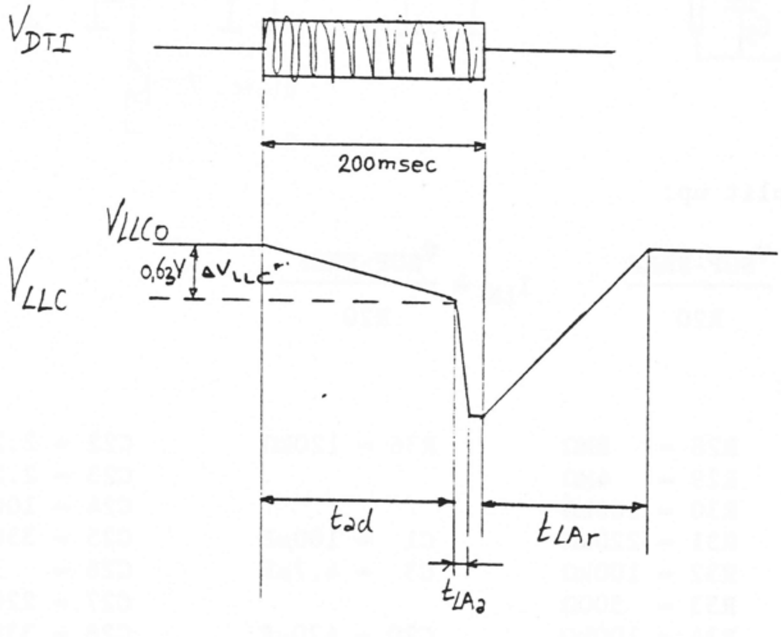
C20 = 470μF
C21 = 68pF

C22 = 2.2μF
C23 = 2.2μF
C24 = 100nF
C25 = 330nF
C26 = 1μF
C27 = 220μF
C28 = 330nF
C31 = 10nF

Fig. 14 Test circuit.
Pins of the TEA1060 that are not shown, are left open.
REMARK: An impedance in series with pin SUP (e.g. an ampmeter) is not allowed because it influences the value of I_{LN}.



a) Listen-in release time (tLIr)
v_{DTI}=100mVrms; f = 3kHz



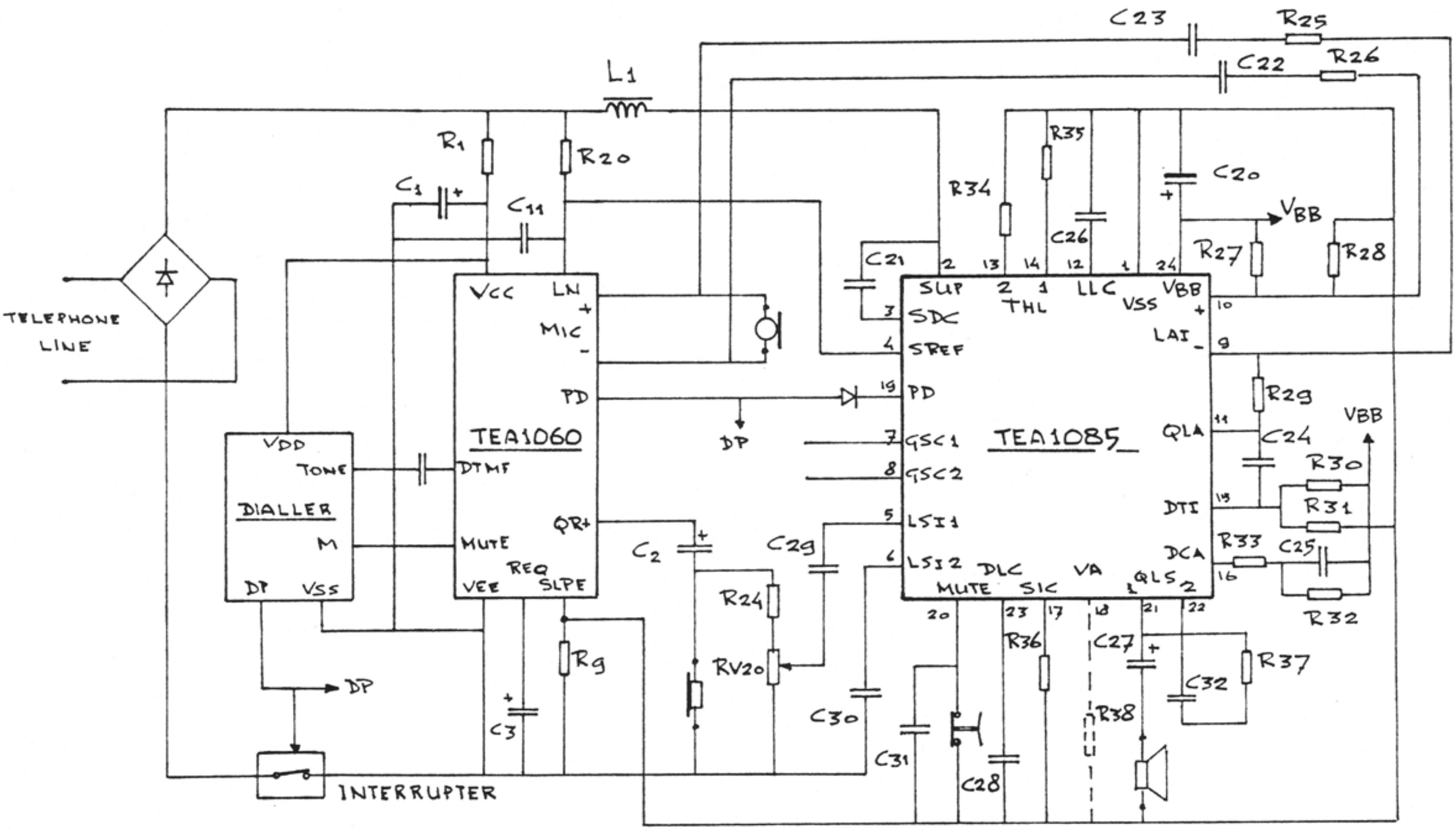
b) Attack delay (tad), Larsen attack time (tLAa),
Larsen release time (tLAr)
v_{DTI}=100mVrms and 1Vrms; f = 3 kHz

Fig. 15 Test signals Larsen Level Limiter

APPLICATION INFORMATION

The basic application circuit is shown in Fig. 16. Only the most important components of the TEA1060 part are shown here. The components that are not shown have values according to the normal application (see TEA1060 data sheet).

REMARK: The supply pin VBB of the TEA1085 can also be used to supply peripheral circuits (e.g. microcontrollers, diallers etc). More information on this will be published in the application report of the TEA1085.



Components values:

R20 = 150Ω
R24 = 1kΩ *
R25 = 10kΩ
R26 = 10kΩ
R27 = 3.3MΩ *
R28 = 3.3MΩ *
R29 =1.65MΩ *
R30 = 100kΩ

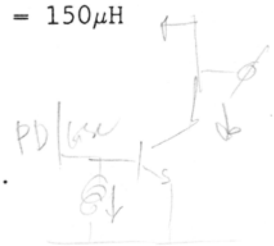
R31 = 220kΩ
R32 = 100kΩ
R33 = 500Ω
R34 = 100kΩ
R35 = 51kΩ
R36 = 120kΩ
R37 = 150Ω
C11 = 4.7nF

C20 = 470μF
C21 = 47pF
C22 = 4.7nF
C23 = 4.7nF
C24 = 4.7nF
C25 = 330nF
C26 = 1μF
C27 = 47μF

C28 = 330nF
C29 = 220nF
C30 = 220nF
C31 = 10nF
C32 = 100nF
R38 : VBB adj.
RV20 = 1kΩ *
L1 = 150μH

*) value depends on gain settings of transmission circuit

Fig. 16. Basic application of TEA1085 together with TEA1060.



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